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DUAL CHIP STACK METHOD FOR ELECTRO-STATIC DISCHARGE PROTECTION OF INTEGRATED CIRCUITS

Background of the Invention

[0001] FIELD OF THE INVENTION

[0002] The present invention relates to the field of integrated circuit chips, particularly the protection of integrated circuit chips from electrostatic discharges.

[0003] BACKGROUND OF THE INVENTION

[0004] Integrated circuits for radio frequency (RF) applications require both active and passive elements. Active elements include metal-oxide-silicon field-effect-transistors (MOSFETs) and bipolar transistors. In RF CMOS (complimentary-metal-oxide-silicon), active elements include N-channel MOSFETs and P-channel MOSFETs. In RF silicon BiCMOS (bipolar-CMOS) technology, active elements include silicon bipolar junction transistors (BJT) in addition to CMOS MOSFETs. In silicon germanium (SiGe) technology, active elements include hetro-junction bipolar transistors (HBT.) For RF circuits both passive and active elements are needed. Examples of passive elements include resistors, capacitors and inductors. In RF applications, passive elements having a high quality factor (Q) are required. High Q capacitors have minimal resistive effects. High Q resistors have low parasitic capacitance. High quality inductors have low series resistance and minimal capacitive coupling to the chip substrate.

[0005]

Typically, high Q passive resistors, capacitors and inductors are placed away from the semiconductor substrate. Inductors, especially, are placed above the chip

interconnect metallurgy to minimize capacitive and inductive coupling to the semiconductor substrate. Inductors are formed from the same materials and processes as used to form the interconnect metallurgy. When a circuit using inductors is required, thick interlevel insulating films and deep vias are used. However, as CMOS interconnect metallurgy scales (linewidth and line thickness decrease) inductor-substrate distance decreases, degrading the Q of the inductor.

[0006] Additionally, electrostatic discharge (ESD) is a phenomenon known to degrade or destroy discrete devices such as transistors, diodes, inductors, capacitors and resistors in integrated circuits. Both voltage and current spikes can break down the dielectric or doped regions in various portions of individual semiconductor devices, thus rending the entire device or even the entire chip completely or partially inoperable.

[0007] Capacitive loading becomes a major concern for integrated circuits running at radio frequencies (RF), i.e. greater than one GHz, as the capacitive loading of conventional ESD devices has an adverse effect on device performance. Conventional ESD devices are large area transistors or diodes fabricated in the semiconductor substrate of the integrated circuit. The capacitance looking into an integrated circuit is given by:

[0008] CTOT = CCKT + CESD (1)

[0009] where: CTOT is the total capacitance of the device;

[0010] CCKT is the capacitance of the integrated circuit; and

[0011] CESD is the capacitance of the ESD protection device.

[0012]

RF circuits are designed with low CCKT values, but ESD protection circuits and devices have relatively high CESD values and the value of CTOT can become dominated by the value of CESD. For example, at one GHz, a CTOT of one pF or less is acceptable. At 10 GHz, CTOT must be about 0.1 pF or less, which is difficult to achieve with conventional ESD protection circuits. At 100 GHz, CTOT must be about 0.01 pF or less, which is very difficult if possible to achieve with conventional ESD protection circuits. ESD protection elements are needed for both active and passive

elements.

[0013] Field emission devices (FEDs)and spark gaps provide ESD protection with little or no added capacitance, but are difficult to implement on semiconductor chips and pose potential contamination and therefore reliability problems. For integrated circuits operating in the RF regime, a method of providing ESD protection is that does not create a reliability problem is needed.

[0014] Therefore, a solution is needed to the problem of providing high Q resistors, capacitors and inductors as CMOS scales smaller as well as a solution to the related problem of providing ESD protection for both the active and passive (especially high Q) elements of RF circuits.

Summary of the Invention

[0015] A first aspect of the present invention is an electronic device comprising: a semiconductor chip including an integrated circuit having at least one electrostatic discharge sensitive device; and a non-semiconductor chip, positioned in close proximity to the semiconductor chip, the non-semiconductor chip having at least one electrostatic discharge protection device, the electrostatic discharge protection device electrically connected to the electrostatic discharge sensitive device.

[0016] A second aspect of the present invention is an electronic device comprising: a semiconductor chip including an integrated circuit; and a non-semiconductor chip, positioned in close proximity to the semiconductor chip, the non-semiconductor chip having at least one electrostatic discharge sensitive device and at least one electrostatic discharge protection device, the electrostatic discharge protection device electrically connected to the electrostatic discharge sensitive device.

[0017] A third aspect of the present invention is an electronic device comprising: a semiconductor chip including an integrated circuit having at least one first electrostatic discharge sensitive device; and a non-semiconductor chip, positioned in close proximity to the semiconductor chip, the non-semiconductor chip having at least one second electrostatic discharge sensitive device and at least one first electrostatic discharge protection device and at least one second electrostatic discharge protection device, the first electrostatic discharge protection device

electrically connected to the first electrostatic discharge sensitive device and the second electrostatic discharge protection device electrically connected to the second electrostatic discharge sensitive device.

[0018] A fourth aspect of the present invention is an electronic device comprising: a dual chip stack comprising: a semiconductor chip including an integrated circuit having at least one electrostatic discharge sensitive device; and a non-semiconductor chip, attached to the semiconductor chip, the non-semiconductor chip having at least one electrostatic discharge protection device, the electrostatic discharge protection device electrically connected to the electrostatic discharge sensitive device.

[0019] A fifth aspect of the present invention is an electronic device comprising: a dual chip stack comprising: a semiconductor chip including an integrated circuit; and a non-semiconductor chip, attached to the semiconductor chip, the non-semiconductor chip having at least one electrostatic discharge sensitive device and at least one electrostatic discharge protection device, the electrostatic discharge protection device electrically connected to the electrostatic discharge sensitive device.

[0020] A sixth aspect of the present invention is an electronic device comprising: a dual chip stack comprising: a semiconductor chip including an integrated circuit having at least one first electrostatic discharge sensitive device; and a non-semiconductor chip, positioned in close proximity to the semiconductor chip, the non-semiconductor chip having at least one second electrostatic discharge sensitive device and at least one first electrostatic discharge protection device and at least one second electrostatic discharge protection device, the first electrostatic discharge protection device electrically connected to the first electrostatic discharge sensitive device and the second electrostatic discharge protection device electrically connected to the second electrostatic discharge sensitive device.

[0021] A seventh aspect of the present invention is an electronic device comprising: a dual chip stack mounted on a module, the dual chip stack comprising: a semiconductor chip including an integrated circuit having at least one electrostatic discharge sensitive device; and a non-semiconductor chip, attached to the semiconductor chip, the non-semiconductor chip having at least one electrostatic discharge protection device, the electrostatic discharge protection device electrically

connected to the electrostatic discharge sensitive device.

[0022] An eighth aspect of the present invention is an electronic device comprising: a dual chip stack mounted on a module, the dual chip stack comprising: a semiconductor chip including an integrated circuit; and a non-semiconductor chip, attached to the semiconductor chip, the non-semiconductor chip having at least one electrostatic discharge sensitive device and at least one electrostatic discharge protection device, the electrostatic discharge protection device electrically connected to the electrostatic discharge sensitive device.

[0023] A ninth aspect of the present invention is an electronic device comprising: a dual chip stack mounted on a module, the dual chip stack comprising: a semiconductor chip including an integrated circuit having at least one first electrostatic discharge sensitive device; and a non-semiconductor chip, positioned in close proximity to the semiconductor chip, the non-semiconductor chip having at least one second electrostatic discharge sensitive device and at least one first electrostatic discharge protection device and at least one second electrostatic discharge protection device, the first electrostatic discharge protection device electrically connected to the first electrostatic discharge sensitive device and the second electrostatic discharge protection device electrically connected to the second electrostatic discharge sensitive device.

[0024] A tenth aspect of the present invention is a method of protecting an electrostatic discharge sensitive component from an electrostatic discharge event comprising: forming the electrostatic discharge sensitive device on a semiconductor chip; forming an electrostatic discharge protection device on a non-semiconductor chip; and electrically connecting the electrostatic discharge sensitive device to the electrostatic discharge protection device.

Brief Description of the Drawings

[0025] The features of the invention are set forth in the appended claims. The invention itself, however, will be best understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawings, wherein:

[0026] FIG. 1 is a side view of a first example of a dual chip stack according to the present invention;

[0027] FIG. 2 is a side view of a second example of a dual chip stack according to the present invention;

[0028] FIG. 3 is a side view of a third example of a dual chip stack according to the present invention;

[0029] FIG. 4 is top view of a spark gap electrostatic discharge protection device according to a first embodiment of the present invention;

[0030] FIGs. 5A through 5D are a partial cross-section views through 5-5 of FIG. 4 illustrating fabrication options of the spark gap/FED electrostatic discharge protection device;

[0031] FIGs. 6A through 6D are a partial cross-section views of the devices illustrated in FIGs. 5A through 5D further illustrating fabrication options of the spark gap/FED electrostatic discharge protection device and including optional dielectric and passivation layers;

[0032] FIG. 7 is top view of a spark gap/FED electrostatic discharge protection device according to a second embodiment of the present invention;

[0033] FIG. 8 is top view of a spark gap/FED electrostatic discharge protection device according to a third embodiment of the present invention;

[0034] FIG. 9 is top view of a spark gap electrostatic discharge protection device according to a fourth embodiment of the present invention;

[0035] FIG. 10 is a partial cross-sectional view of a diode electrostatic discharge device protection device according to a fifth embodiment the present invention;

[0036] FIG. 11 is a partial cross-sectional view of a gated diode electrostatic discharge device protection device according to a sixth embodiment of the present invention;

[0037] FIG. 12 is a top view illustrating a spark gap ESD protection device protecting a wiring pad according to the present invention;

[0038] FIG. 13 is a top view illustrating a spark gap ESD protection device protecting an inductor according to the present invention;

[0039] FIG. 14 is a top view illustrating park gap ESD protection devices protecting a capacitor according to the present invention; and

[0040] FIG. 15 is a top view illustrating spark gap ESD protection devices protecting a thin film resistor according to the present invention.

Detailed Description of the Invention

[0041] FIG. 1 is a side view of a first example of a dual chip stack according to the present invention. In FIG. 1, an integrated circuit chip 100 comprising active semiconductor devices such as transistors and diodes and passive devices such as capacitors, resistors and inductors and circuits thereof, is mounted to a pin grid array (PGA) module 105 having a multiplicity of pins 110. At least a portion of the semiconductor devices contained within integrated circuit chip 100 are sensitive to ESD. The semiconductor devices and circuits contained in integrated circuit chip 100 are electrically connected to PGA module 105 and ultimately to pins 110 by a multiplicity of wirebonds 115. Mounted to integrated circuit chip 100 is a non-semiconductor chip 120 containing a multiplicity of electrostatic discharging devices. Non-semiconductor chip 120 may also contain passive devices such as capacitors, resistors and inductors. The electrostatic discharging devices and capacitors, resistors and inductors contained in non-semiconductor chip 120 are electrically connected to integrated circuit chip 100 by a multiplicity of solder balls 125 which also serve to attach the two chips.

[0042] FIG. 2 is a side view of a second example of a dual chip stack according to the present invention. In FIG. 2, integrated circuit chip 100 comprising active semiconductor devices such as transistors and diodes and passive devices such as capacitors, resistors and inductors and circuits thereof, is mounted to pin grid array (PGA) module 105. At least a portion of the semiconductor devices contained within integrated circuit chip 100 are sensitive to ESD. The semiconductor devices and circuits contained in integrated circuit chip 100 are electrically connected to PGA module 105 and ultimately to pins 110 by a multiplicity of solder balls 130. Mounted

to integrated circuit chip 100 is non-semiconductor chip 120 containing a multiplicity of electrostatic discharging devices. Non-semiconductor chip 120 may also contain passive devices such as capacitors, resistors and inductors. The electrostatic discharging devices and capacitors, resistors and inductors contained in non-semiconductor chip 120 are electrically connected to integrated circuit chip 100 by solder balls 125 which also serve to attach the two chips.

[0043] FIG. 3 is a side view of a third example of a dual chip stack according to the present invention. In FIG. 3, integrated circuit chip 100 comprising active semiconductor devices such as transistors and diodes and passive devices such as capacitors, resistors and inductors and circuits thereof, is mounted to pin grid array (PGA) module 105. At least a portion of the semiconductor devices contained within integrated circuit chip 100 are sensitive to ESD. The semiconductor devices and circuits contained in integrated circuit chip 100 are electrically connected to PGA module 105 and ultimately to pins 110 by a multiplicity of low capacitance RF bumps 135. Mounted to integrated circuit chip 100 is non-semiconductor chip 120 containing a multiplicity of electrostatic discharging devices. Non-semiconductor chip 120 may also contain passive devices such as capacitors, resistors and inductors. The electrostatic discharging devices and capacitors, resistors and inductors contained in non-semiconductor chip 120 are electrically connected to integrated circuit chip 100 by low capacitance RF bumps 140 which also serve to attach the two chips.

[0044] The electrostatic discharging devices contained in non-semiconductor device 120 (and discussed in reference to FIGs. 1, 2 and 3 above) include spark gaps, field emission devices, diodes and gated diodes. The difference between a spark gap and a field emission device is spark gaps generally discharges across an air gap, while a field emission device can discharge across a gap in air, other gas, or a solid such as an insulator. Spark gaps, field emission devices, diodes and gated diodes. and may be used to provide ESD protection for the transistors, diodes, capacitors, resistors and inductors contained in integrated circuit chip 100 as well as the capacitors, resistors and inductors contained in non-semiconductor chip 120 . Integrated circuit chip 100 may comprise a silicon, a silicon on insulator (SOI) or a gallium arsenide substrate. The active devices contained with integrated circuit chip may be fabricated in complementary metal oxide silicon (CMOS), RF CMOS, Bipolar, BiCMOS, SiGe Bipolar,

silicon-germanium-carbon (SiGeC) and SiGe BiCMOS technologies. In one example, non-semiconductor chip 120 is quartz.

[0045] Other types of modules may be used in conjunction with the present invention, including but not limited to ball grid arrays (BGA), surface mount technology (SMT) modules such as small outline packages (SOP), and quad flat packages (QFP) leaderless chip carrier (LCC), tape automated bonded (TAB) modules and other pin type packages . In the case of TAB modules attachment of semiconductor chip 100 to the module is necessarily by bumps and beam leads.

[0046] FIG. 4 is top view of a spark gap electrostatic discharge protection device according to a first embodiment of the present invention. In FIG. 4, an ESD protection device 145 is formed on non-semiconductor substrate 120. ESD protection device 145 comprises a central conductive line 150 having first extending member 155A extending a distance "L1" from a first side 152 of the central conductive line toward a first outer conductive line 160A from a middle portion 165 of the central conductive line. ESD protection device 145 further comprises a second extending member 155B extending from a second side 153, opposite first side 152, of the central conductive line a distance "L2" toward a second outer conductive line 160B. Middle portion 165 is "W" wide. First extending portion 155A tapers to a first tip 170A. First tip 170A is separated from first outer conductive line 160A by a first gap 175A. Second extending portion 155B tapers to a second tip 170B. Second tip 170B is separated from second outer conductive line 160B by a second gap 175B. First gap 175A is "G1" wide and second gap 175B is "G2" wide. A first end 180A of central conductive line 150 is electrically connected to a pad 185 for receiving I/O or other signals. A second end 180B of central conductive line 150 is electrically connected to a circuit or device to be protected. The circuit or device to be protected may reside on non-semiconductor chip 120 or semiconductor chip 100. First outer conductive line 160A is electrically tied to ground (GND) while second outer conductive line 160B is electrically tied to VDD.

[0047] An ESD event occurring on pad 185 will generate a field at either first tip 170A or second tip 170B sufficient to create a current path to either first outer conductive line 160A or second outer conductive line 160B, shunting the ESD event to either outer

conductive line and thus preventing the ESD event from propagating to the circuit or device electrically connected to second end 180B of central conductive line 150.

[0048] Pad 185 and ESD protection device 145 may be integrally formed by in the same conductive layer during fabrication of non-semiconductor chip 120. In one example, ESD protection device 145 is formed from aluminum, aluminum/copper, aluminum/copper/silicon, aluminum/titanium/titanium nitride, copper, copper/tantalum/tantalum nitride or tungsten about 1.0 to 6.0 microns thick. "W" is about 1.0 to 3.0 microns, "L1" and "L2" are 0.5 to 2.0 microns but not necessarily equal and "G1" and "G2" are about 0.5 to 2.0 microns but not necessarily equal. Spark gaps and FEDs fabricated with these values of "W", "L1", "L2", "G1" and "G2" will provide ESD protection for frequencies of about 1.0 to 100 GHz.

[0049] FIGs. 5A through 5D are a partial cross-section views through 5-5 of FIG. 4 illustrating fabrication options of the spark gap/FED electrostatic discharge protection device. In FIG. 5A, electrostatic discharge device 145 is fabricated on a top surface 190 of non-semiconductor chip 120 by, for example, a subtractive etch process.

[0050] In FIG. 5B, electrostatic discharge device 145 is fabricated in a trench 195 formed in non-semiconductor chip 120 by, for example, a damascene process. A top surface 200 of electrostatic discharge device 145 is co-planer with top surface 190 of non-semiconductor chip 120.

[0051] In FIG. 5C, an etch step has been performed on the structure illustrated in FIG. 5B to form a air gap under middle portion 165 of central conductive line 150 and from under a portion of first and second outer conductive lines 160A and 160B in the vicinity of gaps 175A and 175B.

[0052] In FIG. 5D, an insulating layer 178 has been formed on top surfaces 190 and 200 filling gaps 175A and 175B to form a field emission device.

[0053] FIGs. 6A through 6D are a partial cross-section views of the devices of FIGs. 5A through 5D illustrating fabrication options of the spark gap/FED electrostatic discharge protection device and including optional dielectric and passivation layers. In FIG. 6A, electrostatic discharge device 145 is fabricated on top of an optional dielectric layer 210 formed on top surface 190 of non-semiconductor chip 120. An

optional passivation layer 215 is formed on top of central conductive line 150 and first and second outer conductive lines 160A and 160B except near gaps 175A and 175B.

[0054] In FIG. 6B, electrostatic discharge device 145 is fabricated over dielectric layer 215 formed on sidewalls 220 and bottom 225 of trench 195. Optional passivation layer 215 is formed on top of central conductive line 150 and first and second outer conductive lines 160A and 160B except near gaps 175A and 175B.

[0055] In FIG. 6C, an etch step to has been performed, removing a portion of dielectric layer 210 from the structure illustrated in FIG. 6B to form a air gap under middle portion 165 of central conductive line 150 and from under a portion of first and second outer conductive lines 160A and 160B near gaps 175A and 175B. Optional passivation layer 215 is formed on top of central conductive line 150 and first and second outer conductive lines 160A and 160B except near gaps 175A and 175B.

[0056] Dielectric layer 210 may be used to reduce surface leakage otherwise present if central conductive line 150 and inner and outer conductive line are fabricated directly on top surface 190 of non-semiconductor chip 120. In one example, dielectric layer 210 is silicon oxide, silicon nitride or layers thereof.

[0057] In FIG. 6D, an insulating layer 178 has been formed on top surfaces 190 and 200 filling gaps 175A and 175B to form a field emission device.

[0058] FIG. 7 is top view of a spark gap/FED electrostatic discharge protection device according to a second embodiment of the present invention. The only difference between the second embodiment and the first embodiment is that in the second embodiment there are a multiplicity of first tips 170A and a multiplicity of second tips 170B extending from first and second sides 152 and 153 of central conductive line 150 and there are a multiplicity of first and seconds gaps 175A and 175B. Not all of first gaps 170A need be the same width nor all of second gaps 170B need be the same width.

[0059] FIG. 8 is top view of a spark gap/FED electrostatic discharge protection device according to a third embodiment of the present invention. The only difference between the third embodiment and the first embodiment is that in the third

embodiment, both first tip 175A and second tip 175B are on first side 152 of central conductive line 150. Of course, first outer conductive line 160A and second outer conductive line 160B must be positioned on the same side of central conductive line 150.

[0060] FIG. 9 is top view of a spark gap/FED electrostatic discharge protection device according to a fourth embodiment of the present invention. The only difference between the fourth embodiment and the first embodiment is that in the fourth embodiment the first and second outer conductive lines 160A and 160B have pointed first and second concavities 230A and 230B respectively, into which first and second end portions 235A and 235B of middle portion 165 of central conductive line 150 respectively extend into. First end portion 235A extends into first concavity 230A a distance "P1." Second end portion 235B extends into second concavity 230B a distance "P2." "P1" need not be equal to "P2." In one example, "W" is about 1.0 to 3.0 microns, "P1" is about 0.5 to 2.0 microns and "P2" is about 0.5 to 2.0 microns and "G1" is about 0.5 to 2.0 microns and "G2" is about 0.5 to 2.0 microns. Spark gaps fabricated with these values of "W", "P1", "P2", "G1" and "G2" will provide ESD protection for frequencies of about 1.0 to 100 GHz.

[0061] While diodes may not be suitable for high frequency protection, their inclusion on non-semiconductor chip 120 is useful for protection of lower frequency circuits that may be present in semiconductor chip 100.

[0062] FIG. 10 is a partial cross-sectional view of a diode electrostatic discharge device protection device according to a fifth embodiment of the present invention. In FIG. 10, a dielectric layer 240 is formed on top surface 190 of non-semiconductor chip 120. A polysilicon diode 245 has been formed on top of dielectric layer 240. Diode 245 comprises an N+ region 250 formed on a first side 252 of an intrinsic region 255 and a P+ region 260 formed on a second side 262 of the intrinsic region. In one example, N region 250 is doped to a concentration of about 1020 atom/cm3 and P region 260 is doped to a concentration of about 1020 atom/cm3. Dielectric layer 240 improves leakage characteristics of diode 245 and allows a higher quality polysilicon to be formed. A first conductive wire 250A is electrically connected to P region 260 by a first silicide region 255A. A second conductive wire 250B is electrically connected to

N+ region 250 by a second silicide region 255B.

[0063] FIG. 11 is a partial cross-sectional view of a gated diode electrostatic discharge device protection device according a sixth embodiment of the present invention. In FIG. 11, dielectric layer 240 is formed on top surface 190 of non-semiconductor chip 120. A gated polysilicon diode 260 has been formed on top of dielectric layer 240. Gated diode 260 comprises an N+ region 265 formed on a first side 267 of a PÌ... region 270 and a P+ region 275 formed on a second side 277 of the PÌ... region. In one example, N+ region 265 is doped to a concentration of about 1020 atom/cm3, P+ region 275 is doped to a concentration of about 1020 atom/cm3 and PÌ... region 270 is doped to a concentration of about 1016 atom/cm3. Dielectric layer 240 improves leakage characteristics of gated diode 260 and allows a higher quality polysilicon to be formed. A first conductive wire 280A is electrically connected to P+ region 275 by a first silicide region 285A. A second conductive wire 280B is electrically connected to N+ region 265 by a second silicide region 285B. Formed over PÌ... region 270 is a gate dielectric 290 and formed on the gate dielectric is a gate conductor 295.

[0064] FIG. 12 is a top view illustrating a spark gap ESD protection device protecting a wiring pad according to the present invention. In FIG. 12, on non-semiconductor chip 120, an ESD protection device 300 is a spark gap protection device and is connected between an I/O pad 305 and an inter-chip pad 310 by a central conductive line 315 of the ESD protection device. In the present example, pads 305 and 310 are integral with central conductive line 315. Inter-chip pad 310 is used to electrically connect ESD protection device 300 contained on non-semiconductor chip 120 to active or passive devices contained in semiconductor chip 100 in order to protect those devices from ESD events. In one example, ESD protection device 300 and pads 305 and 310 are formed from aluminum, aluminum/copper, aluminum/copper/silicon, aluminum/titanium/titanium nitride, copper, copper/tantalum/tantalum nitride or tungsten about 1.0 to 6.0 microns thick.

[0065]

FIG. 13 is a top view illustrating a spark gap ESD protection device protecting an inductor according to the present invention. In FIG. 13, on non-semiconductor chip 120, an ESD protection device 300 is a spark gap protection device and is connected

to an inductor 320 by central conductive line 315 of the ESD protection device. Inductor 320 is comprised of a planer coil 325 and a tap 330. In the present example, coil 325 is integral with central conductive line 315 and formed in a first level of wiring. Tap 330 is formed in a second wiring level separated from the first wiring level by an interlevel dielectric and connected to coil 325 by via 335. An optional window 340 is formed in the interlevel dielectric layer to provide an air gap spark gap.

[0066] Inductor 320 and ESD protection device 300 may be connected to circuits contained in semiconductor chip 100 in order to provide those circuits with high Q inductors that are also protected from ESD events. The inductor is a High Q inductor because an inductor built on non-semiconductor chip 120 can have lower parasitic capacitance and resistance compared to one built on semiconductor chip 100 and provided with conventional ESD protection.

[0067] In one example, ESD protection device 300 and inductor 320 (including tap 330) are formed from aluminum, aluminum/copper, aluminum/copper/silicon, aluminum/titanium/titanium nitride, copper, copper/tantalum/tantalum nitride or tungsten about 1.0 to 6.0 microns thick.

[0068] FIG. 14 is a top view illustrating spark gap ESD protection devices protecting a capacitor according to the present invention. In FIG. 14, on non-semiconductor chip 120, a pair of ESD protection devices 300 (each being a spark gap protection device) are connected to opposite plates of capacitor 345 by the central conductive line of the each of the ESD protection devices. A lower plate 350A of capacitor 345 is connected to first ESD protection device 300A by central conductive line 315A of the first ESD protection device. First ESD protection device 300A and lower plate 350A are integrally formed in a first wiring level. An upper plate 350B of capacitor 345 is connected to second ESD protection device 300B by central conductive line 315B of the second ESD protection device. Second ESD protection device 300B and upper plate 350B are integrally formed in a second wiring level. The first and second wiring levels are separated by an interlevel dielectric layer. An optional window 340 is formed in the interlevel dielectric layer to provide an air gap spark gap. Capacitor 345 and first and second ESD protection devices 300A and 300B may be connected to circuits contained in semiconductor chip 100 in order to provide those circuits with high Q

capacitors that are also protected from ESD events. Capacitor 345 is a high Q capacitor because first and second ESD protection devices 300A and 300B do not reduce the Q of the capacitor.

[0069] In one example, first and second ESD protection devices 300A and 300B and first and second plates 350A and 350B are formed from aluminum, aluminum/copper, aluminum/copper/silicon, aluminum/titanium/titanium nitride, copper, copper/tantalum/tantalum nitride or tungsten about 1.0 to 6.0 microns thick and the interlevel dielectric is formed from silicon oxide, silicon nitride or layers thereof.

[0070] FIG. 15 is a top view illustrating spark gap ESD protection devices protecting a thin film resistor according to the present invention. In FIG. 15, on non-semiconductor chip 120, a pair of ESD protection devices 300 (each being a spark gap protection device) are connected to opposite ends of resistor 355 by the central conductive line of the each of the ESD protection devices. A first end 360A of resistor 355 is connected to first ESD protection device 300A by central conductive line 315A of the first ESD protection device. A second end 355B of resistor 355 is connected to second ESD protection device 300B by central conductive line 315B of the second ESD protection device. First and second ESD protection devices 300A, 300B, and resistor 355 are integrally formed in the same wiring level. In actuality, first and second central conductive lines 315A and 315B are one continuous conductive wire and resistor 355 is a narrow region of that continuous wire. Resistor 355 and first and second ESD protection devices 300A and 300B may be connected to circuits contained in semiconductor chip 100 in order to provide those circuits with high Q resistors that are also protected from ESD events. Resistor 355 is a high Q resistor because first and second ESD protection devices 300A and 300B do not reduce the Q of the resistor.

[0071] In one example, first and second ESD protection devices 300A and 300B and thin film resistor 355 are formed from aluminum, aluminum/copper, aluminum/copper/silicon, aluminum/titanium/titanium nitride, copper, copper/tantalum/tantalum nitride or tungsten about 1.0 to 6.0 microns.

[0072] While a spark gap/FED, and particularly the spark gap/FED device of the first embodiment has been illustrated in FIGs. 12 through 15 and described above, any of the spark gap/FED or diode ESD protection device embodiments described in FIGs. 4

through 12 and described above may be substituted. Further, a high quality dielectric such as silicon oxide, silicon nitride or layers thereof may be provided on top surface 190 of non-semiconductor chip 120 to reduce leakage of the protect devices, inductors, capacitors and resistors.

[0073] The description of the embodiments of the present invention is given above for the understanding of the present invention. It will be understood that the invention is not to the particular embodiments described herein, but is capable of various modifications, rearrangements and substitutions as will now become apparent to those skilled in the art without departing from the scope of the invention. Therefore it is intended that the following claims cover all such modifications and changes as fall within the true spirit and scope of the invention.